Amendments to the Claims:

Please amend claim 1 as follows. Please cancel claims 4 and 26-37 as follows.

The listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1. (Currently Amended) A method of fabricating a metal-oxide semiconductor (MOS) transistor having an elevated source/drain structure, comprising:

forming a gate dielectric on an active region of a semiconductor substrate and forming a gate electrode on the gate dielectric;

forming a first gate spacer on lateral side surfaces of the gate electrode;

following formation of the first gate spacer, forming a first epi-layer on the semiconductor substrate;

ion-implanting a dopant in the first epi-layer and in the semiconductor substrate to form a source/drain extension region in the semiconductor substrate after forming the first epi-layer;

following formation of the source/drain extension region, forming a second gate spacer on lateral side surfaces of the first gate spacer; [[and]]

following formation of the second gate spacer, forming a second epi-layer on the first epi-layer; and

ion implanting a dopant in the second epi-layer, in the first epi-layer and in the semiconductor substrate to form a deep source/drain region below the source drain extension region in the semiconductor substrate after forming the second epi-layer.

2. (Original) The method as set forth in claim 1, further comprising:

forming a first gate oxide on the lateral side surfaces of the gate electrode before the first gate spacer is formed; and

forming a second gate oxide on the lateral side surfaces of the first gate spacer before the second gate spacer is formed.

3. (Original) The method as set forth in claim 1, further comprising:

forming a first poly-layer on the gate electrode while the first epi-layer is formed; and

forming a second poly-layer on the first poly-layer while the second epi-layer is formed.

4. (Cancelled)

5. (Original) The method as set forth in claim 1, wherein a thickness of the first epi-layer is about 20 to 30 % of a combined thickness of an elevated source/drain layer formed by the first epi-layer and the second epi-layer.

6. (Original) The method as set forth in claim 1, wherein a thickness of the second epi-layer is about 70 to 80 % of a combined thickness of an elevated source/drain layer formed by the first epi-layer and the second epi-layer.

7. (Original) The method as set forth in claim 1, wherein the second gate spacer is four to six times wider than the first gate spacer.

8. (Original) The method as set forth in claim 1, wherein at least one of the first epi-layer and second epi-layer comprises silicon.

9. (Original) The method as set forth in claim 8, wherein at least one of the first epi-layer and second epi-layer is grown in accordance with a low pressure chemical vapor deposition process.

10. (Original) The method as set forth in claim 9, wherein at least one of the first epi-layer and second epi-layer is formed using a source gas including dichlorosilane and HCl.

11. (Original) The method as set forth in claim 9, wherein the low pressure chemical vapor deposition process is conducted under 10 to 30 torr.

12. (Original) The method as set forth in claim 8, wherein at least one of the first epi-layer and second epi-layer is grown in accordance with an ultra-high vacuum chemical vapor deposition process.

13. (Original) The method as set forth in claim 12, wherein at least one of the first epi-layer and second epi-layer is formed using a source gas, including $Si_2H_6$.

14. (Original) The method as set forth in claim 12, wherein the ultra-high vacuum chemical vapor deposition process is conducted under $10^{-4}$ to $10^{-5}$ torr.

15. (Original) The method as set forth in claim 8, further comprising:

baking the semiconductor substrate or the first epi-layer at 800 to 900°C under a hydrogen atmosphere for one to five minutes before the at least one of the first epi-layer and second epi-layer is formed.

16. (Original) The method as set forth in claim 1, wherein at least one of the first epi-layer and second epi-layer comprises silicon-germanium.

17. (Original) The method as set forth in claim 16, wherein at least one of the first epi-layer and second epi-layer is grown in accordance with a low pressure chemical vapor deposition process.

18. (Original) The method as set forth in claim 17, wherein at least one of the first epi-layer and second epi-layer is formed using a source gas, including dichlorosilane, HCl, and $GeH_4$.

19. (Original) The method as set forth in claim 17, wherein the low pressure chemical vapor deposition process is conducted under 10 to 30 torr.

20. (Original) The method as set forth in claim 16, wherein at least one of the first epi-layer and second epi-layer is grown in accordance with a ultra-high vacuum chemical vapor deposition process.

21. (Original) The method as set forth in claim 20, wherein at least one of the first epi-layer and second epi-layer is formed using a source gas, including dichlorosilane, HCl, and $GeH_4$.

22. (Original) The method as set forth in claim 20, wherein the ultra-high vacuum chemical vapor deposition process is conducted under $10^{-4}$ to $10^{-5}$ torr.

23. (Original) The method as set forth in claim 16, further comprising:

baking the semiconductor substrate or the first epi-layer at 800 to 900°C under a hydrogen atmosphere for one to five minutes before the first epi-layer or second epi-layer is formed.

24. (Original) The method as set forth in claim 1, further comprising forming a source/drain layer by in-situ doping a dopant in at least one of the first epi-layer and second epi-layer during forming the first epi-layer or second epi-layer.

25. (Original) The method as set forth in claim 1, further comprising forming a source/drain layer by ion-implanting a dopant in at least one of the first epi-layer or second epi-layer during forming the first epi-layer or second epi-layer.

26.-37. (Cancelled)